REMARKS

Claims 2, 4, 6, 7, 9, 10, 12, 13, 15-17, 20, 22, 24, 25, 27-29, and 34-38 are pending in the present application.

In the office action mailed December 1, 2004 (the "Office Action"), claims 2-7, 9-13, 15-18, and 32-39 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,357,621 to Cox (the "Cox patent") in view of U.S. Patent No. 6,070,231 to Ottinger (the "Ottinger patent"). Claims 20-25 and 27-30 were also rejected in the Office Action under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,160,562 to Chin *et al.* (the "Chin patent") in view of the Cox patent and in view of the Ottinger patent.

Claims 3, 5, 11, 18, 21, 23, 30, 32, 33, and 39 have been cancelled by amendment. Consequently, the rejection of these claims by the Examiner is now moot.

Before discussing the rejection of the pending claims, the disclosed embodiments of the invention will now be discussed in comparison to the applied references in order to help the Examiner appreciate certain distinctions between the pending claims and the subject matter of the applied references. Specific distinctions between the pending claims and the references will be discussed after the discussion of the disclosed embodiment and the references. This discussion of the differences between the disclosed embodiment and the applied references does not define the scope or interpretation of any of the claims.

Embodiments of the present invention are directed to a memory system that allows faulty blocks of memory to be ignored during memory access and enable the otherwise functional memory blocks of the memory to be used. As described in the present application, for the particular embodiment of the present invention represented in Figures 3a-c, an embedded memory 220 includes an embedded memory array 308 segmented into four memory blocks 334, 338, 342, and 346. A memory controller 216 includes a register 304 having fields 312, 316, 320, 324, and 330. One register field stores a value that is indicative of the number of functional blocks of memory. The same value, as shown in Figures 3a-c, is indicative of which of the blocks of memory are functional. The register 304 further includes four BANK fields, 316, 320, 324, and 330. Each BANK field corresponds to one of the four blocks of memory 334, 338, 342, and 346. When the memory is accessed, the values stored in the register 304 are referenced to access the corresponding physical memory location of the memory blocks 334, 338, 342, 346.

Figure 5 of the present application illustrates another embodiment of the present invention. The memory subsystem 500 has a distributed memory controller arrangement that is represented by registers 504 and 554. Each of the registers 504 and 554 are located in a respective memory controller. Two memory controllers which are coupled together through a memory controller bus are included in the memory subsystem 500. The memory controller bus allows memory access requests, as well as data, to be passed between the two memory controllers. The memory subsystem 580 further includes memory arrays 508 and 558, each of which is segmented into (M+1) and (N+1) memory blocks, respectively. The register 504 includes start address field 512, memory size field 514 to define the range of addressable memory coupled to the memory controller having the register 504. The register 504 further includes a memory valid field 516 and (M+1) BANK fields 518-526. Each of the BANK fields 518-526 corresponds to one of the (M+1) memory blocks in the memory array 508. The register 554 includes fields similar to the register 504. Namely, the register 554 includes a start address field 562 and memory size field 564 to define the memory coupled to the memory controller having the register 554. The register 554 further includes a memory valid field 566 and BANK fields 568-574. Each of the BANK fields 568-574 corresponds to one of the memory blocks in the memory array 558. The memory valid fields 516 and 566 store a value indicative of the number of functional memory blocks of the respective memory array. The value of each of the valid fields is shown in Figure 500 further indicates which of the memory blocks of the respective memory arrays are functional. The BANK fields 518-526 and 568-574 store values indicating which blocks of memory are assigned to a respective memory bank.

The Examiner has characterized the Cox patent as teaching all of the limitations of claims 4, 10, 16, 35, and 37, "except for a memory controller bus coupled between a first and second memory controllers for passing memory access request [sic] from one memory controller to another memory controller." *See* the Office Action at page 3. However, as discussed in detail in the previously filed responses on March 5, 2003 (the "First Response"), August 28, 2003 (the "Second Response"), and January 20, 2004 (the "Third Response"), the Cox patent does not disclose the combination of limitations as characterized by the Examiner. In addition to the discussion in the First, Second, and Third Responses, the Cox patent further fails to disclose the memory controllers and registers as recited in claims 4, 10, 16, 35, and 37.

For example, claim 4 recites a memory subsystem that includes a first memory controller having a first register having at least M+1 register fields, a first of the register fields storing a value indicative of the number of functional memory sub-arrays of the first memory array, and M register fields each for storing a value indicative of which of the M sub-arrays correspond to the respective blocks of memory and further includes a second memory controller having a second register having at least N+1 register fields, a first of the register fields storing a value indicative of the number of functional memory sub-arrays of the second memory array, and N register fields each for storing a value indicative of which of the N sub-arrays correspond to the respective blocks of memory.

The Cox patent does not disclose the first and second memory controllers as recited in claim 4. The Examiner makes reference to the Memory Address Mask command (Opcode 40-4F), described in the Cox patent at col. 10, lines 1-37, as disclosing values to keep track of the number of functional sub-arrays in the memory module. The Opcode, however, is not a value that is indicative of the number of functional blocks of memory, either explicitly or implicitly. As stated in the Cox patent, the 0 to F hexadecimal values of the mask command values define the absolute *starting block address* of a memory module. *See* col. 10, lines 6-9. That is, the Memory Address Mask command for each of the modules must be different in order for the memory system to function correctly, since the value is used in determining the address ranges of the memory modules. In contrast, the value stored in the valid fields as recited in claim 4 can theoretically be the same for each of the memory arrays because the value is indicative of the number of functional blocks of the memory array. Where two different memory arrays having the same total number of memory blocks and memory capacity have the same memory block failing, the value stored in the registers of each of the memory controllers coupled to the two different memory arrays will have the same value stored. This cannot occur for the memory system described in the Cox patent since the Memory Address Mask command is used for defining the starting address of a memory module. If two different modules have the same Memory Address Mask command value, that is, the same start address, the memory system would not know which of the memory modules to access for a memory address falling in the overlapping address range of the two memory modules. Thus, the Memory Address Mask

command value is not analogous to the stored value indicative of the number of functional blocks of memory, as recited in claim 4.

Additionally, the Memory Address Mask command value for a memory does not implicitly provide the number of functional blocks of memory for the memory module. As previously discussed, the Memory Address Mask command value for a memory module is used for defining the beginning address of the memory module, and does not take into account the number of functional blocks of the particular memory module. This is demonstrated by the fact that the Memory Address Mask command value for a memory module will be exactly the same regardless of the number of functional blocks of that memory module. The value does not change even if the number of functional blocks of that memory module changes. Clearly, the Memory Address Mask command value does not implicitly provide the number of functional blocks of memory for that memory module.

Moreover, the Cox patent fails to disclose storing values in register fields that are indicative of which of the memory sub-arrays correspond to the respective blocks of memory, unlike claim 4. The Cox patent describes a memory system that bypasses failed memory blocks of memory modules based on the starting address assigned to each of the memory modules by the system controller 11. *See* col. 5, lines 22-54. By setting the starting addresses of each of the memory modules appropriately, undefined blocks or space corresponding to failed memory blocks of that memory module can be bypassed. In contrast to the limitations recited in claim 4, the system described in the Cox patent does not disclose storing values in register fields of a register that are indicative of which blocks of memory of a memory array correspond to which banks defined in the register.

With respect to claim 10, claim 10 recites a memory subsystem including, among other things, a first register to store pointer values directing access to each functional sub-array, the first register having a first field for storing data indicative of the number of functional memory sub-arrays of the first memory array, and further having M fields for storing data indicative of which of the M memory sub-arrays are assigned to a respective memory bank and a second register to store second pointer values directing access to each functional sub-array of the second memory array, the second register having a first field for storing data indicative of the number of functional memory sub-arrays of the first memory array, and further having N fields

for storing data indicative of which of the N memory sub-arrays are assigned to a respective memory bank. The number of fields of the register, in addition to a field storing data indicative of the number of functional memory sub-arrays, corresponds to the number of blocks of memory of a respective memory array.

With respect to claim 16, claim 16 recites a memory subsystem that includes a first memory controller coupled to access the first memory array and having a register including at least M+1 data fields, one data fields storing a value indicative of which memory sub-arrays of the first memory array are functional and M fields for storing a value indicative of which memory sub-arrays to access in response to the first memory controller receiving a memory access request and a second memory controller coupled to access the second memory array and having a register including at least N+1 data fields, one data fields of the register storing a value indicative of which memory sub-arrays of the second memory array are functional and N fields for storing a value indicative of which memory sub-arrays to access in response to the second memory controller receiving a memory access request.

Claim 35 recites a method of accessing a memory array including storing a first value indicative of the number of functional sub-arrays of the memory array and indicative of which of the M memory sub-arrays are functional, and storing for each memory block a value indicative of which of the M memory sub-arrays corresponds to the respective memory block. Claim 37 recites a method of accessing an embedded memory array including storing a value indicative of the number of functional memory sub-arrays of the memory array and which of M memory sub-arrays are functional and storing for each of a plurality of memory blocks a pointer value identifying which of the M memory sub-arrays are assigned thereto.

As previously discussed with respect to claim 4, the Cox patent fails to describe a the memory controller or register as recited in claims 10 and 16, and the method of storing the values recited in claims 35 and 37. For example, the Cox patent fails to disclose a register that stores data indicative of the number of functional memory sub-arrays of a respective memory array. The Cox patent also fails to describe the register storing data indicative of which of the memory sub-arrays are assigned to which memory banks. Additionally, the Cox patent does not disclose that the Memory Address Mask command is indicative of which of the blocks of memory are functional. The Cox patent uses values to define the starting address of a memory

module, such as the Memory Address Mask command (Opcode 40-4F) referenced by the Examiner. The Memory Address Mask command value does not provide the number of functional blocks for a memory module, either explicitly or implicitly, as previously described with respect to claim 4. Moreover, the Memory Address Mask command value is not indicative of which of the blocks of memory of a memory array correspond to which of the banks of memory defined in a register. Failed memory blocks are bypassed in the Cox system by defining the starting addresses of each memory module accordingly, and not by storing values that identify the association of the blocks of memory of a memory array to banks of memory.

The Examiner has cited the Ottinger patent as teaching "a memory controller bus coupled between a first and second memory controller for passing memory access request from one memory controller to another memory controller." *See* the Office Action at page 3. Even if the Examiner's characterization of the Ottinger patent is considered accurate, the teachings fail to make up for the deficiencies of the Cox patent previously described with respect to claims 4, 10, 16, 35, and 37. Although the Examiner has characterized the use of a first MLST 28 and second MLST 28b as storing information that is utilized in determining whether a memory request is to be issued to a second memory controller, *see id.*, this however, does not teach or suggest the storing of a value indicative of the number of functional blocks of a memory array, or storing values indicative of the correspondence between the functional blocks of the memory array and memory banks.

Consequently, the combined teachings of the Cox patent in view of the Ottinger patent do not teach or suggest the combination of limitations recited in claims 4, 10, 16, 35, and 37. For the foregoing reasons, claims 4, 10, 16, 35, and 37 are patentable over the Cox patent in view of the Ottinger patent. Claims 2, 6, and 7, which depend from claim 4, claims 9, 12, and 13, which depend from claim 10, claims 15 and 17, which depend from claim 16, claims 34 and 36, which depend from claim 35, and claim 38, which depends from claim 37, are similarly patentable based on their dependency from a respective allowable base claim. Therefore, the rejection of claims 2, 4, 6, 7, 9, 10, 12, 13, 15-17, and 34-38 under 35 U.S.C. 103(a) should be withdrawn.

In rejecting claims 20-25 and 27-30 under 35 U.S.C. 103(a), the Examiner has cited the Chin patent as teaching a computer having all of the limitations of claims 22 and 28

except the first memory and the second memory with faulty sub-arrays being left unassigned, and first and second memory controllers coupled to receive memory access requests, and a memory controller bus coupled between the first and second memory controllers to pas memory request from one memory controller to another. *See* page 5 of the Office Action. The combination of the Cox patent in view of the Ottinger patent has been cited by the Examiner as teaching the elements lacking from the Chin patent.

Claim 22 is directed to a graphics processing system having a memory subsystem similar to that recited in claim 4. Claim 28 is directed to a computer system that includes a graphics processing system recited in claim 22. However, as previously discussed, the combination of the teachings of the Cox and Ottinger patents fails to teach or suggest memory subsystems recited by claims 2, 4, 6, 7, 9, 10, 12, 13, 15-17, and 34-38. Consequently, the Cox and Ottinger patents fail to make up for the deficiencies of the Chin patent. Therefore, the rejection of claims 20, 24, 25, and 27-29 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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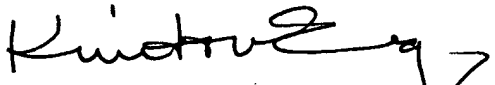

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